0.3-6.0GHz GaN Power Amplifier

Product Introduction

HX430006C1 is a GaN HEMT transistor based on the high-power amplifier chip is made of GaN power MMIC process.The operating frequency range covers 0.3GHz ~ 6GHz, with large power gain 10dB, typical saturated output power 10W, power added efficiency greater than 35%, can work in pulse and continuous wave mode.Through-hole grounding, dual power supply operation, typical operating voltage Vd=+28V, Vg=-2.6V.

Key technical parameters

Frequency range: 0.3GHz~6.0GHz

Power gain: 10dB

Saturated output power: 40dBm

Power added efficiency: 35%

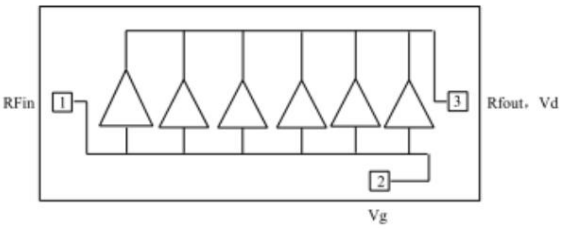
Power supply: +28V@ 500mA (static)

Chip size: 3.30 mm × 2.40 mm × 0.10 mm

Application

Microwave transceiver components

High power solid state transmitter



HX430006C1 Functional Block Diagram

Maximum Ratings

parameter	symbol	Limit value
Maximum drain-source forward bias voltage	Vd	+32V
Minimum gate negative bias	Vg	-5V
Maximum input power	Pin	+33dBm
Storage temperature	Top	-65℃～+150℃
Operating temperature	Top	-55℃～+125℃

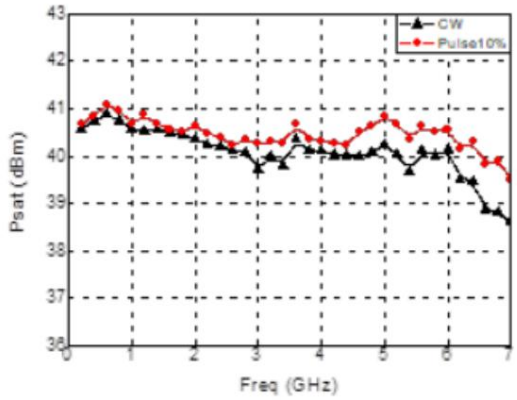
Main electrical parameters (TA = +25℃,Vd = +28V)

index	symbol	Minimum	Typical Value	Maximum	unit
Frequency range	f		0.3~6		GHz
Saturated output power	Psat	40	40.5	41	dBm
Power Gain	Gp	10	11	12	dB
Power gain flatness	△Gp	·	·	±0.5	dB
Power Added Efficiency	PAE	35	40	·	%
Linear gain	Gain	16	16.5	17	dB
Linear gain flatness	△Gain	·	·	±0.5	dB
Dynamic drain current	Idd	·	0.9	1.3	A

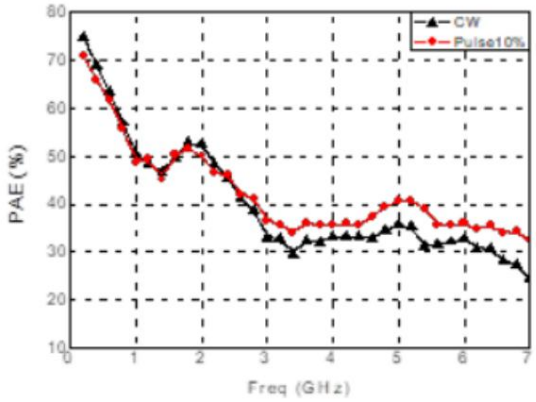
Note: All chips have been 100% DC tested and 100% RF tested on-chip.

Typical curve (Vd=+28V, Vg=-2.6V)

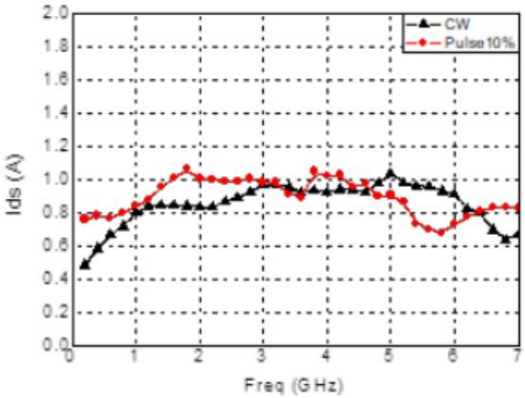
Saturated output power vs. frequency (Pin=30dBm)



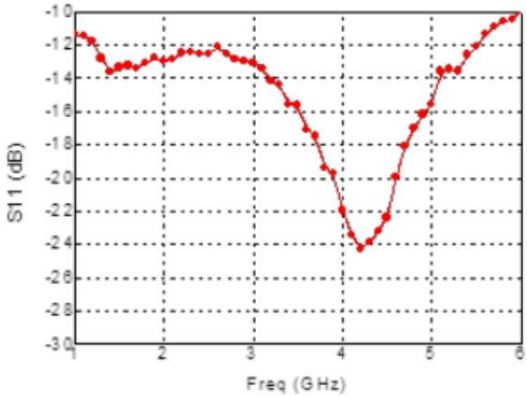
Additional efficiency vs. frequency (Pin=30dBm)



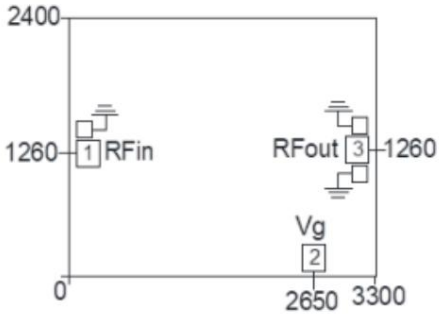
Dynamic current vs. frequency (Pin=30dBm)

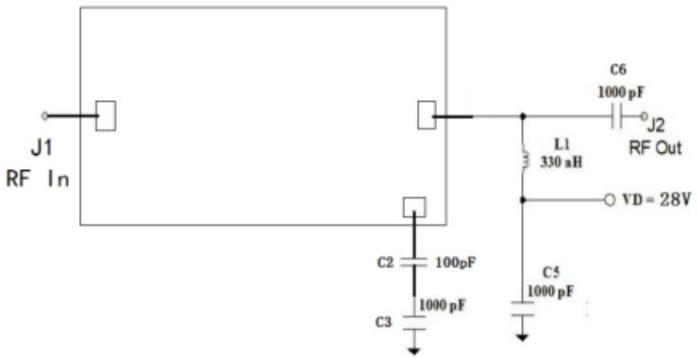


Input standing wave vs. frequency (Pin=-10dBm)



Dimensions and typical applications





Note:

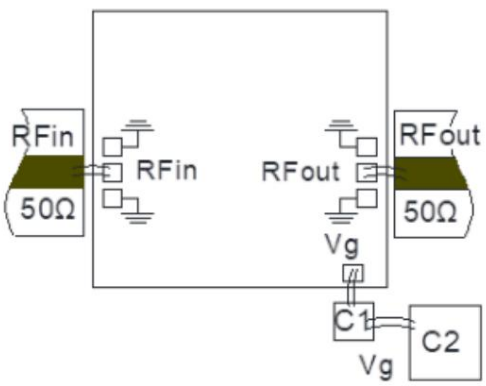
The units in the figure are all micrometers (μm);
Chip thickness 80μm;
Dimension tolerance: ±50μm.

illustrate:
External DC blocking capacitors and bias circuits will affect chip performance.
Please select devices appropriately according to the frequency band you are using.

Pressure point arrangement diagram

number	symbol	Function	Size
1	RFin	Signal input terminal	100μm×100μm
2	Vg	Gate power supply terminal	100μm×100μm
3	RFout, Vd	signal output terminals, external DC blocking capacitors and bias inductors are required	100μm×100μm

Recommended assembly drawing



Note: The capacitance of the external capacitor is C1=100pF, C2=1000pF.

Precautions

1. The single-chip circuit needs to be stored in a dry and clean N2 environment;
2. The chip substrate 6H-SiC material is very brittle and must be used with care to avoid damaging the chip;
3. There is no insulating protective layer on the chip surface, so attention should be paid to the cleanliness of the assembly environment to avoid excessive contamination of the surface;
4. The thermal expansion coefficient of the carrier should be close to that of 6H-SiC material, with a linear thermal expansion coefficient of 4.2×10-6/℃,It is recommended that the carrier material be CuMoCu， or CuW; or CuMo：
5. Avoid holes between the chip and the carrier during assembly, and ensure good heat dissipation between the box and the carrier;6. It is recommended to use gold-tin solder for sintering, Au:Sn=80%:20%, sintering temperature not exceeding 300 ℃，time not longer than 30 seconds, and sintering process to avoid high temperature rapid changes require gradual temperature rise and fall;
7. It is recommended to use gold wire with a diameter of 25μm to 30μm, the temperature of the bonding platform chassis should not exceed 250℃， the bonding time should be as short as possible, and the bonding process should avoid high temperature Rapid changes;
8. The chip has a DC-blocking capacitor inside the input, and the output needs to be connected to an external bias inductor and DC-blocking capacitor;
9. When powering on, first increase the gate voltage and then the drain voltage. When powering off, first reduce the drain voltage and then the gate voltage.
10. Pay attention to anti-static during chip use and assembly, wear grounded anti-static bracelets, and ensure that the sintering and bonding stations are well grounded;