1. Functional Topology

The Ku band four-channel T/R SiP module integrates four transceiver channels. Each channel includes a 6-bit digital control phase shifter, a 6-bit digital control attenuator (no attenuation in transmit mode), and a transmit/receive amplifier. The functional topology of the module is shown in Figure 1.

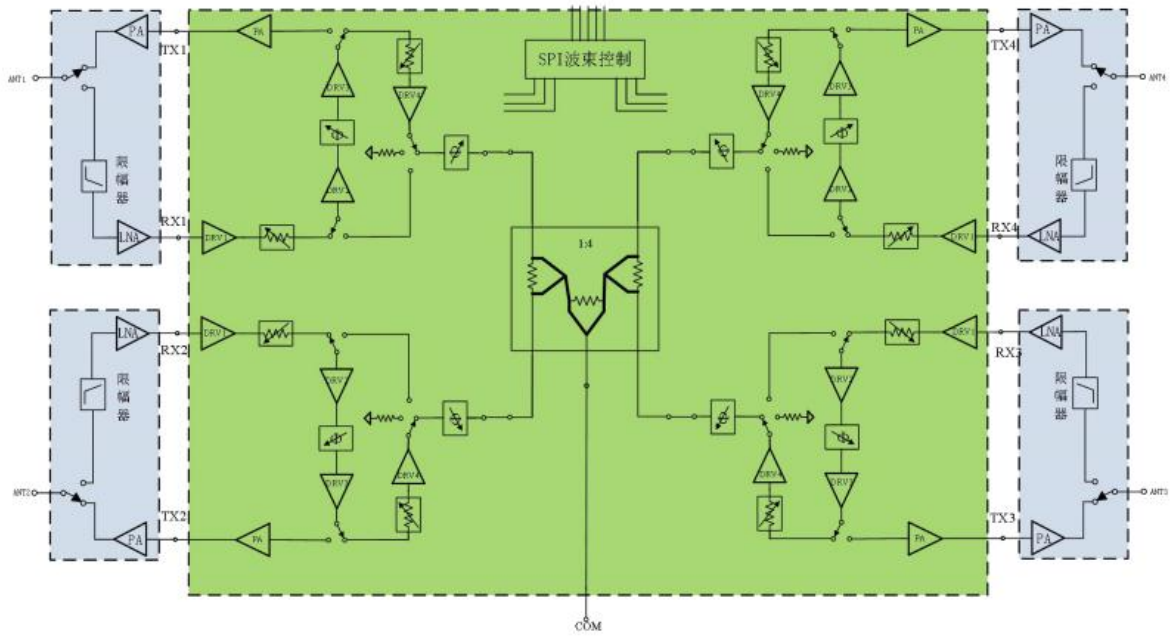


Figure 1 SiP Module Functional Topology

2. Performance Specifications

2.1 Operating Conditions

a) Operating Frequency: 14 GHz ~ 18 GHz;

b) Power Supply Voltages: +6V, -5V, +3.3V

c) Maximum Transmit Duty Cycle: 25%

d) Maximum Transmit Pulse Width: 100 us

e) Transmit Input Power: 4 dBm

2.2 Electrical Characteristics

Table 1 Electrical Characteristics

Parameter	Test Conditions: f=14~18 GHz, -55℃≤TA≤85℃	Min	Max	Unit	Remarks
Transmit Channel	Transmit Pulse Peak PowerTA=25℃	33	-	dBm	
	In-Band Power Flatness	-0.8	+0.8	dB	
	Output Power Consistency (TA=25℃)	-0.5	+0.5	dB	Inter-channel at same frequency
	Transmit Phase Shift Bits	6	–	bit	
	Transmit Phase Shift Accuracy (RMS, TA=25℃)	–	5	°	
	Output Pulse Rise Time (TA=25℃)	–	100	ns	With 120μF external capacitor, batch sampling
	Output Pulse Fall Time (TA=25℃)	–	100	ns	
	Transmit Pulse Droop (TA=25℃)	–	0.8	dB	
	Initial Phase Consistency (TA=25℃)	-30	+30	°	Inter-channel at same frequency
	Spurious Suppression (10M-40G, TA=25℃)	60	–	dBc	Batch sampling
	Harmonic Suppression (TA=25℃)	25	–	dBc	Batch sampling
	Single-Channel Transmit Peak Current@+6V/+3.3V	—	1300/90	mA	
Receive	Noise Figure (TA=25℃)	–	4	dB	

Channel	Receive GainTA=25℃	25	——	dB	
	Gain Flatness	-1.5	+1.5	dB	
	Receive Gain Consistency (TA=25℃)	-1.5	+1.5	dB	Inter-channel at same frequency
	Initial Phase Consistency (TA=25℃)	-30	+30	°	Inter-channel at same frequency
	Phase Shift Bits	6	–	bit	
	Receive Phase Shift Accuracy (RMS, TA=25℃)	–	5	°	
	Amplitude Degradation in Different Phase States (TA=25℃)	-1.5	+1.5	dB	
	Attenuation Bits	6	–	bit	
	Receive Attenuation Accuracy (RMS)	—	1.0	dB	
	Phase Change in Different Attenuation States (RMS, TA=25℃)	–	5	°	
	Power Modulation Rise Time (TA=25℃)	–	50	ns	Batch sampling
	Power Modulation Fall Time (TA=25℃)	–	50	ns	
	Receive Input VSWR (TA=25℃)	–	2.5	–	
	Receive Output VSWR (TA=25℃)	–	1.8	–	

	Single-Channel Receive Peak Current@+3.3V/-5V	—	70/20	mA	
	Module Efficiency (TA=25℃)	23	–	%	25% transmit duty cycle, 75% receive duty cycle
	No Self-Excitation in Tx/Rx	–	Pass	–	-55℃~85℃

2.3 Design Assurance Specifications

a) Phase Shift Switching Time: ≤0.1 us;

b) Tx/Rx Switching Time: ≤0.2 us;

c) Transmit VSWR Tolerance: Withstands full reflection for 5 min, output power change ≤0.3 dB;

d) Receive Channel Input P-1: ≥-35 dBm;

e) Channel Isolation: ≥40 dB;

f) Receive Channel Maximum Input Power: 2W CW ;

3. Packaging

The module adopts an integrated package substrate design with BGA surface-mount device packaging.

4. Materials and Components

1. 100% domestic for packaging raw materials.
2. Internal RF components use microwave MMIC devices with 100% domestic localization rate.

5. Physical Interface

The module uses a BGA interface design. The BGA pin layout is shown in Figure 2.

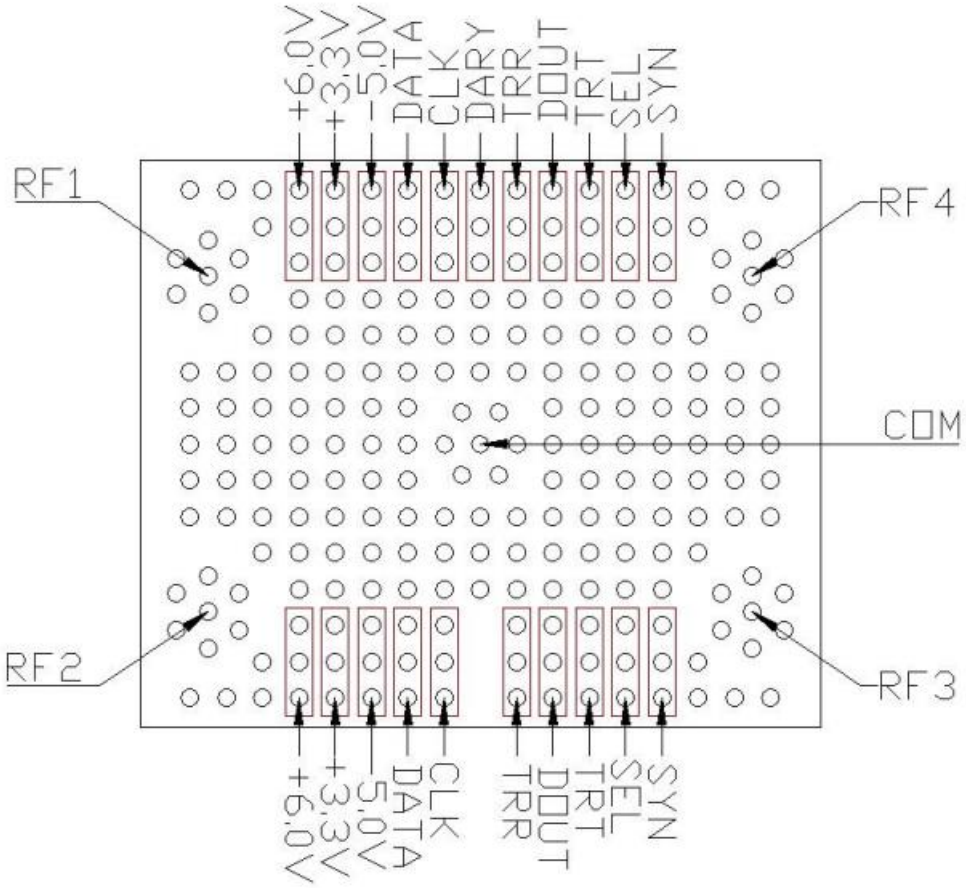


Figure 2 BGA Interface Layout (Perspective View)

Table 2 BGA Interface Function Definitions

Symbol	Attribute	Function Description
DOUT	Output	Serial data output
CLK	Input	Clock
DATA	Input	Serial data input
SEL	Input	Chip select signal
TRR	Input	Receive modulation pulse signal
TRT	Input	Transmit pulse modulation signal
DARY	Input	Primary latch signal

SYN	Input	Secondary latch signal (waveform refresh)
+3.3V	Input	+3.3V power supply
-5V	Input	-5V power supply
+6V	Input	+6V power supply
RF1	I/O	Channel 1 input/output port
RF2	I/O	Channel 2 input/output port
RF3	I/O	Channel 3 input/output port
RF4	I/O	Channel 4 input/output port
COM	I/O	Common input/output port
(Blank)	Ground	Ground

6. Power Interface

Table 3 Module Power Requirements

Voltage	Transmit Peak Current (A)	Receive Peak Current (A)	Typical Average Current (A, 25% Tx duty cycle)
+6V	5	0.003	1.25
-5V	0.02	0.02	0.02
+3.3V	0.28	0.25	0.26

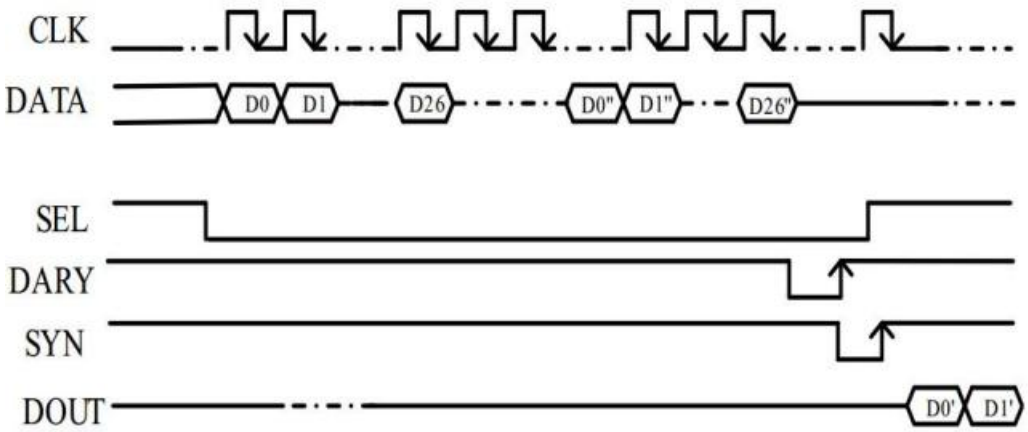
7. Control Interface

Each transceiver channel of the SiP module has 27-bit serial data, with a total of 108 bits for four channels. The functional definition of each 27-bit data field per channel is shown in Table 4.

Table 4 Serial Data Bit Mapping for Transceiver Channels

模式	R	T	N/A	发射移相（1 有效）						接收移相（1 有效）						N/A						接收衰减（1 有效）					
数据位	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
5.625	0	1	x	1	0	0	0	0	0							x	x	x	x	x	x						
11.25	0	1	x	0	1	0	0	0	0							x	x	x	x	x	x						
22.5	0	1	x	0	0	1	0	0	0							x	x	x	x	x	x						
45	0	1	x	0	0	0	1	0	0							x	x	x	x	x	x						
90	0	1	x	0	0	0	0	1	0							x	x	x	x	x	x						
180	0	1	x	0	0	0	0	0	1							x	x	x	x	x	x						
5.625	1	0	x							1	0	0	0	0	0	x	x	x	x	x	x						
11.25	1	0	x							0	1	0	0	0	0	x	x	x	x	x	x						
22.5	1	0	x							0	0	1	0	0	0	x	x	x	x	x	x						
45	1	0	x							0	0	0	1	0	0	x	x	x	x	x	x						
90	1	0	x							0	0	0	0	1	0	x	x	x	x	x	x						
180	1	0	x							0	0	0	0	0	1	x	x	x	x	x	x						
0.5	1	0	x													x	x	x	x	x	x	1	0	0	0	0	0
1	1	0	x													x	x	x	x	x	x	0	1	0	0	0	0
2	1	0	x													x	x	x	x	x	x	0	0	1	0	0	0
4	1	0	x													x	x	x	x	x	x	0	0	0	1	0	0
8	1	0	x													x	x	x	x	x	x	0	0	0	0	1	0
16	1	0	x													x	x	x	x	x	x	0	0	0	0	0	1

Figure 3 Control Timing Diagram for Amplitude-Phase Multifunctional Chip (Single/Parallel Operation)



Notes:

1. DATA is serial input, shifted on CLK falling edge with LSB first. 27 bits per channel, 108 bits total for four channels (channel order: 4/3/2/1).
2. DOUT is serial output of shift register; leave pin floating if unused.
3. SEL is active low for serial data input.
4. DARY is primary data latch signal, active on rising edge.
5. SYN is secondary data latch signal (waveform refresh), active on rising edge.

Table 5 Module Operating State Logic Table

Inputs				Outputs			
TRT	TRR	D1	D0	TX	RX	LOAD	State
0	1	x	1	0	1	0	Receive
1	0	1	x	1	0	0	Transmit
x	x	0	0	0	0	1	Load

8. Dimensions

6. Module Body Dimensions: 15mm × 12.5mm × 2.8mm, tolerance ±0.15mm
7. BGA Ball Type: High-lead solder balls, diameter 0.5mm

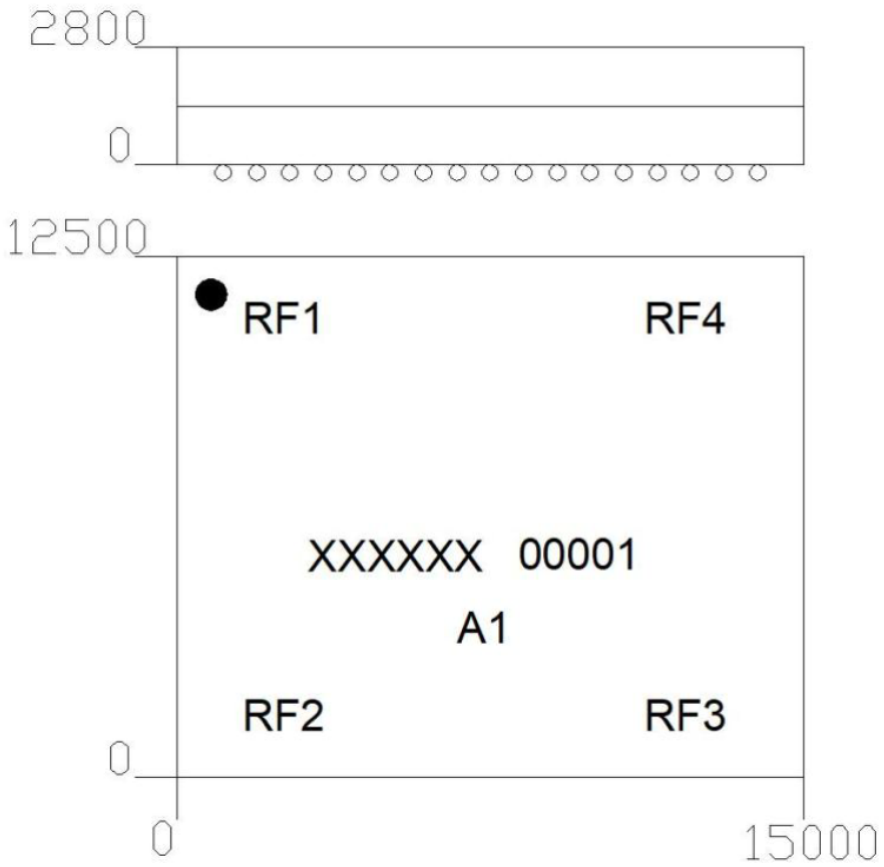


Figure 4 SiP Module Outline Drawing

9. Weight

Module weight ≤ 2.5 grams.

10. Appearance

8. Top cover surface gold-plated.

9. Substrate sidewalls and bottom non-balled areas: Bare packaging material.

11. Markings and Codes

The front of the cover has the following markings:

a) Model: xxxx

b) Manufacturer Code: xx

c) Lot Identification Code: 6-digit date code (e.g., 231301)

d) Unique Serial Number: 5-digit sequence (e.g., 00001)

e) Orientation Mark: Solid dot at RF port 1 output corner

f) Port Labels: RF1~RF4 for RF output ports

g) Test Equipment Code: Alphanumeric combination (e.g., A1)

12. Environmental Adaptability

a) Storage Temperature: -55℃ ~ +85℃

b) Operating Temperature: -55℃ ~ +85℃