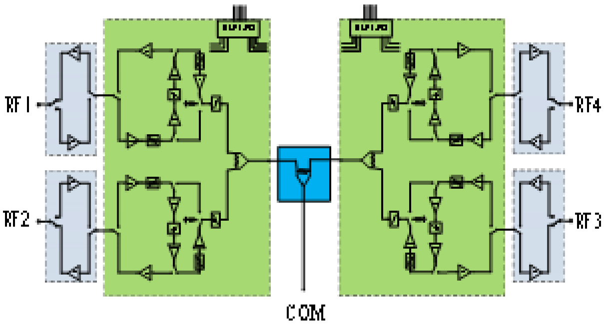
Performance Characteristics

- -Frequency Range: 8GHz - 12GHz;
- - Receive Gain: 22dB;
- - Noise Figure: 3dB;
- - Transmit Power Gain: 28dB;
- - Transmit Saturation Power: 37dBm;
- - 6-bit Phase Shifter RMS：5°;
- - 6-bit Attenuator RMS ： 1.2dB;
- - TTL-level Serial Control;
- - Module Size: 16mm×16mm×3.4mm (excluding balls);

Principle Block Diagram



Product Introduction

HX9X4010G16 is an X-band surface-mount four-channel transceiver module. It adopts the BGA packaging form. The shell is made of ceramic substrate, and the enclosure and cover are made of metal materials. The thermal resistance of the module is reduced by means of heat dissipation from the top and the bottom simultaneously. The module integrates the following circuit functions: 6-bit numerically controlled phase shifter, 6-bit attenuator, transmit driver amplifier, receive low-noise amplifier, power divider, switch circuit, and serial-to-parallel driver, etc. The operating frequency ranges from 8GHz to 12GHz. The receive gain is 20dB, the noise figure is 3dB, the transmit output saturation power is 37dBm, and the transmit power gain is 28dB. This module is mainly applied to microwave transceiver components to achieve functions such as amplification, amplitude modulation, and phase modulation of transceiver signals.

Electrical Parameters

When the transmit channel and the receive channel are working, Vd1 = +28V, Vd2 = +3.3V, Vee1=-5V，Vee2=-28V. The following are the single-channel indicate:

Parameter Name	Parameter Name	Test Conditions Pulse Width 50us Duty Cycle 5% f = 8 -12GHz	Minimum Value	Typical Value	Maximum Value	Unit
Transmit Channel	Transmit Gain	TA = 25°C	-	28	-	dB
	Gain Flatness	TA = 25°C	-1	-	1	dB
	Saturation Power	TA = 25°C	-	37	-	dBm
	Input Port VSWR	TA = 25°C	-	1.5	-	
	Number of Phase Shifting Bits	TA = 25°C	6bit, 5.625°	6bit, 5.625°	6bit, 5.625°	

	RMS of 64-phase Shifting States	TA = 25℃	-	5	-	°
	Phase Shifting Amplitude Variation	TA = 25℃	-1	-	1	dB
	Channel Gain Consistency	TA = 25℃	-0.5	-	0.5	dB
	Channel Phase Consistency	TA = 25℃	-30	-	30	°
	VD1 Current	TA = 25℃	-	650	-	mA
	VD2 Current	TA = 25℃	-	350	-	mA
	Vee1 Current	TA = 25℃	-	1.5	-	mA
Receive Channel	Noise Figure	TA = 25℃	-	3.0	-	dB
	Receive Gain	TA = 25℃	-	22	-	dB
	Gain Flatness	TA = 25℃	-1	-	1	dB
	Input P-1	TA = 25℃	-	-27	-	dBm
	Input Port VSWR	TA = 25℃	-	1.3	-	
	Number of Phase Shifting Bits	TA = 25℃	6bit, 5.625°	6bit, 5.625°	6bit, 5.625°	
	RMS of 64-phase Shifting States	TA = 25℃	-	2.5	-	°
	Phase Shifting Amplitude Variation	TA = 25℃	-1.5	-	1.5	dB
	Number of Attenuation Bits	TA = 25℃	6 bit, 0.5dB	6 bit, 0.5dB	6 bit, 0.5dB	
	RMS of 64 Attenuation States	TA = 25℃	-	1	-	dB
	Additional Phase Shift of Attenuation	TA = 25℃	-10	-	10	°

	Channel Gain Consistency	TA = 25℃	-1	-	1	dB
	Channel Phase Consistency	TA = 25℃	-30	-	30	°
	Vd1 Current	TA = 25℃	-	0	-	mA
	Vd2 Current	TA = 25℃	-	95	-	mA
	Vee1 Current	TA = 25℃	-	1.5	-	mA

Operating Limit Parameters

Parameter	Symbol	Limit Value
Maximum Drain-Source Voltage 1	Vd1	+32V
Maximum Drain-Source Voltage 2	Vd2	+4V
Minimum Driver Supply Voltage	Vee	-5.5V
Maximum Input Power (RF1/RF2/RF3/RF4)	Pin(200us, 20%)	+40dBm
Maximum Input Power (COM)	Pin	+15dBm
Storage Temperature	TSTG	-55°C to +85°C
Operating Temperature	Top	-55°C to +85°C

Registers in the beam control circuit can be classified into five categories according to their functions, as shown in the following table:

Register			Name	Definition
Register Status	reg_shift		Status Shift Register	Shift register, containing amplitude - phase and transmit - receive control data for each channel
	reg_data	reg_data1	Status Data Register 1	The first - stage latch, with 32 sets of registers for each channel. The read - write address is determined by reg_fun2

		reg_data2	Status Data Register 2	The second - stage latch
Register Control	reg_fun1		Control Shift Register	Shift register, writing the read - write address bit data of reg_data1
	reg_fun2		Control Data Register	Stores the read - write address data of reg_data1, with 16 sets of registers

Definition of the Control Register Structure

There are 16 control data registers (reg_fun2), and each register contains 8 - bit data, as shown in the following table. Only the lower 5 - bit of the first two control data registers are used in this protocol, corresponding to the write and read addresses of the status data register 1 (reg_data1) respectively.

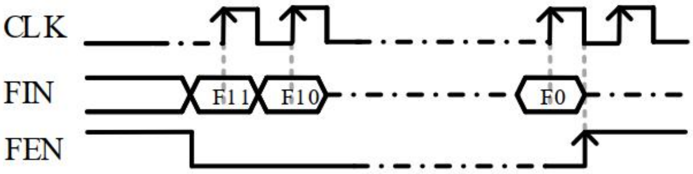
reg_fun2	D7	D6	D5	D4	D3	D2	D1	D0	Explanation
reg_fun2[0]	-	-	-	reg2_addr_w[4:0]					Write address bit selection
reg_fun2[1]	-	-	-	reg2_addr_r[4:0]					Read address bit selection
reg_fun2[2] - [15]	Internally reserved								

The control shift register (reg_fun1) contains read - write address bit control signals. reg_fun1 contains 12 - bit data, where addr is the high 4 - bit of reg_fun1, representing the address of the control data register (reg_fun2), and data is the low 8 - bit of reg_fun1, representing the data written into the corresponding reg_fun2.

Control Shift Register	11	…	8	7	…	0
Content Definition	addr			data		

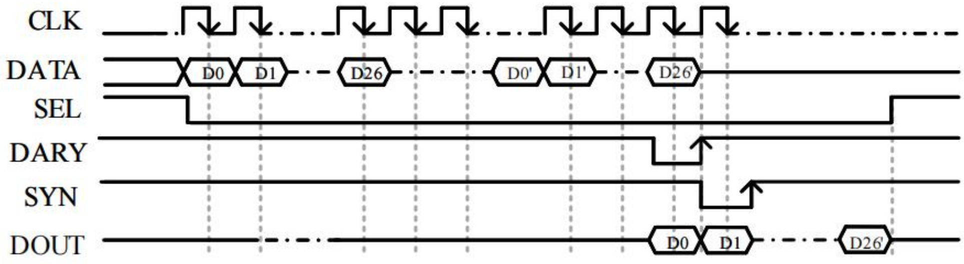
When configuring the control register, when FEN is at a low level, on the rising edge of CLK, the FIN input signal will be sequentially written into reg_fun1[0], and the original data in reg_fun1 will be sequentially shifted from reg_fun1[0] to reg_fun1[11]. reg_fun1 will write the data in data into the specified position in reg_fun2 according to the value of addr. For example, when addr is 0x1, data will be written into reg_fun2[1].

The basic functions of the SPI interface protocol rely on eight interfaces: CLK, SEL, DATA, DARY, SYN, DOUT, FIN, and FEN. CLK is the system synchronization clock, FIN is the serial input signal of the control shift register, and FEN is a low - level - effective enable signal. When FEN is low, on the rising edge of CLK, the FIN serial input signal is stored in the control shift register (reg_fun1) until all 12 - bit signals are stored. At this time, the FEN signal is pulled high, and on the first rising edge of CLK after being pulled high, the 12 - bit data is written into the control data register (reg_fun2). The write timing diagram of the control register is as follows:

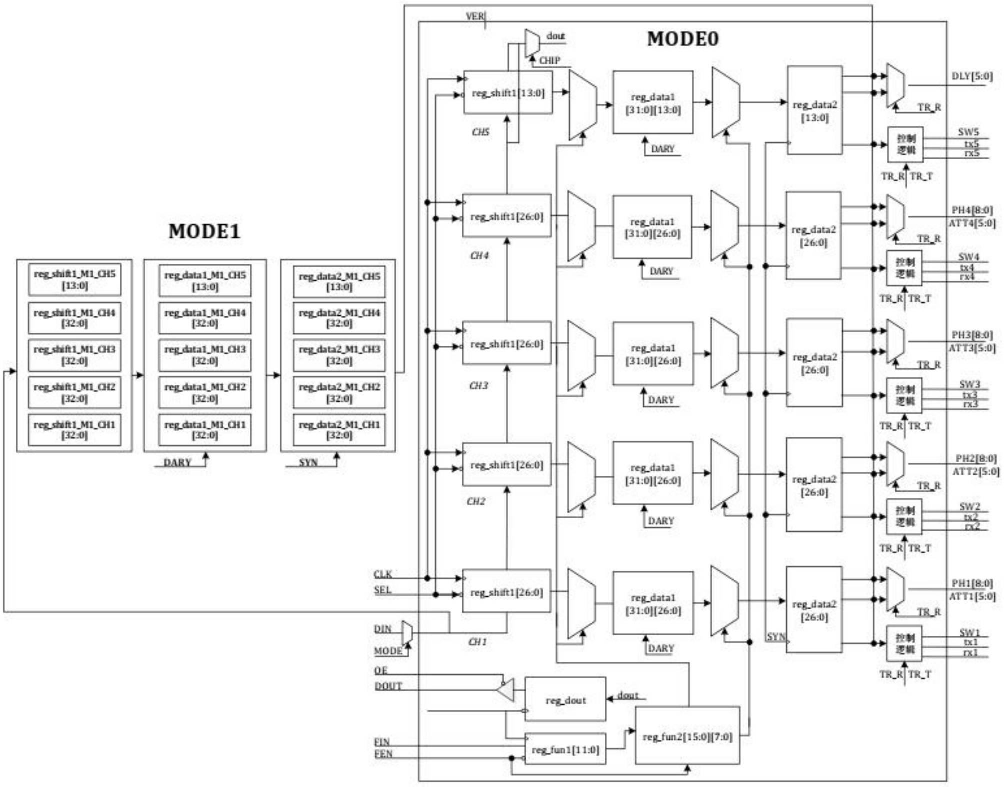


SEL is a low - level - effective chip select synchronization signal, DATA is the serial input signal of the status shift register (reg_shift), and DOUT is the serial output signal of the status shift register (reg_shift). The input of DATA and the output of DOUT are both at the falling edge of CLK when SEL is at a low level, and the writing and output are in groups of the complete data of all channels. When the SEL signal changes from high to low, the chip is selected, and the serial input signal of DATA starts to be stored in the status shift register until all signals are stored. At this time, DOUT starts to output the first - bit serial input signal.

After the DATA data is written, on the rising edge of DARY, the serial data is written into the status data register 1 (reg_data1), and the write address bit of reg_data1 is determined by the control data register (reg_fun2). On the rising edge of SYN, the data in reg_data1 is read out to the status data register 2 (reg_data2), and the read address bit of reg_data1 is determined by reg_fun2. After the data is output through reg_data2, it passes through a multiplexer with TR_R as the selection signal to output the transmit - receive amplitude - phase and switch control signals. The write and read timing of the status register is as follows. It should be noted that the serial write operation after power - on should be completed after the power - on reset delay (between 20 - 60us).



Block Diagram of the Beam Control Circuit is as following:



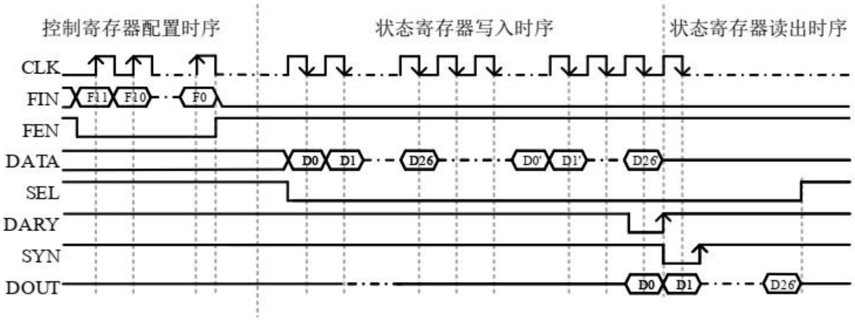
1. reg_shift1_CHx (x = 1 - 4) is the status shift register. At the falling edge of CLK, if SEL is 0, the shift starts. The data enters reg_shift1_CH1 from the DATA port and starts to shift. The data in reg_shift1_CH1[26] starts to shift towards reg_shift1_CH1[0], and the value of reg_shift1_CH1[0] is shifted to reg_shift1_CH2[26] (that is, the first - input data is the lowest - bit reg_shift1_CH5[0] of channel 5), and the same rule applies to channels 2, 3, 4, and 5.

2. reg_data1_CHx (x = 1 - 4) is the status data register 1, corresponding to the previous - stage reg_shift1_CHx respectively. Each channel's reg_data1_CHx has 32 sets of registers, namely reg_data1_CHx[31] - reg_data1_CHx[0]. On the rising edge of DARY, all the data in reg_shift1_CHx will be written into reg_data1_CHx specified by reg_fun2[0][4:0].

3. reg_data2_CHx (x = 1 - 4) is the status data register 2, corresponding to the previous - stage reg_shift1_CHx and reg_data1_CHx respectively. On the rising edge of SYN, the data selected by reg_fun2[1][4:0] in reg_data1_CHx will be read out to reg_data2_CHx.

4. After the data is output through reg_data2_CHx, it passes through a multiplexer with TR_R as the selection signal to output the transmit - receive amplitude - phase and switch control signals.

Timing Diagram of Function Register Configuration



The single - read - write control timing diagram is as shown above.

1. First configure the read - write address bits in the control register.
2. When configuring the control register, pull the SEL signal high; when configuring the status register, pull the FEN signal high to avoid data misalignment or incorrect storage.

Truth Table

The module's serial data has 122 bits. In the module, each of channels 1 - 4 has 27 bits, and the common channel has 14 bits.The function definitions of the data bits are shown in the following table.

Delay Channel	Delay Channel	Channel 4	Channel 4	Channel 3	Channel 3	Channel 2	Channel 2	Channel 1	Channel 1
D0	Receive Enable Control Bit	D14	Receive Enable Control Bit	D41	Receive Enable Control Bit	D68	Receive Enable Control Bit	D95	Receive Enable Control Bit
D1	Transmit Enable Control Bit	D15	Transmit Enable Control Bit	D42	Transmit Enable Control Bit	D69	Transmit Enable Control Bit	D96	Transmit Enable Control Bit
D2	Set to 0	D16	Set to 0	D43	Set to 0	D70	Set to 0	D97	Set to 0
D3	Set to 0	D17	Transmit Phase Shift Control Bit 5.625°	D44	Transmit Phase Shift Control	D71	Transmit Phase Shift Control	D98	Transmit Phase Shift Control

					Bit 5.625°		Bit 5.625°		Bit 5.625°
D4	Set to 0	D18	Transmit Phase Shift Control Bit 11.25°	D45	Transmit Phase Shift Control Bit 11.25°	D72	Transmit Phase Shift Control Bit 11.25°	D99	Transmit Phase Shift Control Bit 11.25°
D5	Set to 0	D19	Transmit Phase Shift Control Bit 22.5°	D46	Transmit Phase Shift Control Bit 22.5°	D73	Transmit Phase Shift Control Bit 22.5°	D100	Transmit Phase Shift Control Bit 22.5°
D6	Set to 0	D20	Transmit Phase Shift Control Bit 45°	D47	Transmit Phase Shift Control Bit 45°	D74	Transmit Phase Shift Control Bit 45°	D101	Transmit Phase Shift Control Bit 45°
D7	Set to 0	D21	Transmit Phase Shift Control Bit 90°	D48	Transmit Phase Shift Control Bit 90°	D75	Transmit Phase Shift Control Bit 90°	D102	Transmit Phase Shift Control Bit 90°
D8	Set to 0	D22	Transmit Phase Shift Control Bit 180°	D49	Transmit Phase Shift Control Bit 180°	D76	Transmit Phase Shift Control Bit 180°	D103	Transmit Phase Shift Control Bit 180°
D9	Set to 0	D23	Receive Phase Shift Control Bit 5.625°	D50	Receive Phase Shift Control Bit 5.625°	D77	Receive Phase Shift Control Bit 5.625°	D104	Receive Phase Shift Control Bit 5.625°
D10	Set to 0	D24	Receive Phase Shift Control Bit 11.25°	D51	Receive Phase Shift Control Bit 11.25°	D78	Receive Phase Shift Control Bit 11.25°	D105	Receive Phase Shift Control Bit 11.25°
D11	Set to 0	D25	Receive Phase Shift Control Bit	D52	Receive Phase Shift	D79	Receive Phase Shift	D106	Receive Phase Shift

			22.5°		Control Bit 22.5°		Control Bit 22.5°		Control Bit 22.5°
D12	Set to 0	D26	Receive Phase Shift Control Bit 45°	D53	Receive Phase Shift Control Bit 45°	D80	Receive Phase Shift Control Bit 45°	D107	Receive Phase Shift Control Bit 45°
D13	Set to 0	D27	Receive Phase Shift Control Bit 90°	D54	Receive Phase Shift Control Bit 90°	D81	Receive Phase Shift Control Bit 90°	D108	Receive Phase Shift Control Bit 90°
		D28	Receive Phase Shift Control Bit 180°	D55	Receive Phase Shift Control Bit 180°	D82	Receive Phase Shift Control Bit 180°	D109	Receive Phase Shift Control Bit 180°
		D29	Transmit Attenuation Control Bit 0.5dB	D56	Transmit Attenuation Control Bit 0.5dB	D83	Transmit Attenuation Control Bit 0.5dB	D110	Transmit Attenuation Control Bit 0.5dB
		D30	Transmit Attenuation Control Bit 1dB	D57	Transmit Attenuation Control Bit 1dB	D84	Transmit Attenuation Control Bit 1dB	D111	Transmit Attenuation Control Bit 1dB
		D31	Transmit Attenuation Control Bit 2dB	D58	Transmit Attenuation Control Bit 2dB	D85	Transmit Attenuation Control Bit 2dB	D112	Transmit Attenuation Control Bit 2dB
		D32	Transmit Attenuation Control Bit 4dB	D59	Transmit Attenuation Control Bit 4dB	D86	Transmit Attenuation Control Bit 4dB	D113	Transmit Attenuation Control Bit 4dB
		D33	Set to 0	D60	Set to 0	D87	Set to 0	D114	Set to 0
		D34	Set to 0	D61	Set to 0	D88	Set to 0	D115	Set to 0

		D35	Receive Attenuation Control Bit 0.5dB	D62	Receive Attenuation Control Bit 0.5dB	D89	Receive Attenuation Control Bit 0.5dB	D116	Receive Attenuation Control Bit 0.5dB
		D36	Receive Attenuation Control Bit 1dB	D63	Receive Attenuation Control Bit 1dB	D90	Receive Attenuation Control Bit 1dB	D117	Receive Attenuation Control Bit 1dB
		D37	Receive Attenuation Control Bit 2dB	D64	Receive Attenuation Control Bit 2dB	D91	Receive Attenuation Control Bit 2dB	D118	Receive Attenuation Control Bit 2dB
		D38	Receive Attenuation Control Bit 4dB	D65	Receive Attenuation Control Bit 4dB	D92	Receive Attenuation Control Bit 4dB	D119	Receive Attenuation Control Bit 4dB
		D39	Receive Attenuation Control Bit 8dB	D66	Receive Attenuation Control Bit 8dB	D93	Receive Attenuation Control Bit 8dB	D120	Receive Attenuation Control Bit 8dB
		D40	Receive Attenuation Control Bit 16dB	D67	Receive Attenuation Control Bit 16dB	D94	Receive Attenuation Control Bit 16dB	D121	Receive Attenuation Control Bit 16dB

Notes:

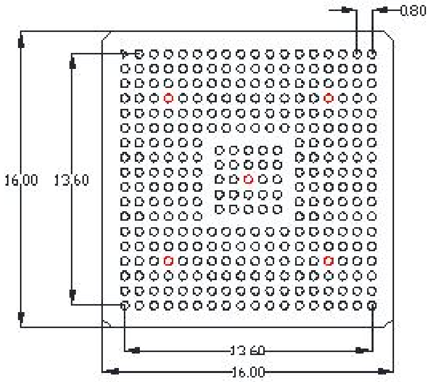
1)The data bit D0 is first-in, first-out.

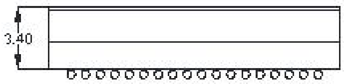
2)The amplitude-phase and attenuation control bits are active at high level, and the delay control bits are active at low level. The delay state is positive delay.

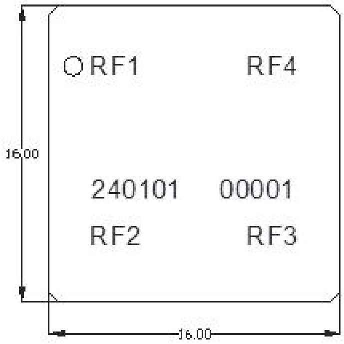
3)The transmit-receive control states are shown in the following table.

TR1	TR2	Transmit Enable Bit	Receive Enable Bit	State
1	0	x	1	Receive State
0	1	1	x	Transmit State
Others				Load State

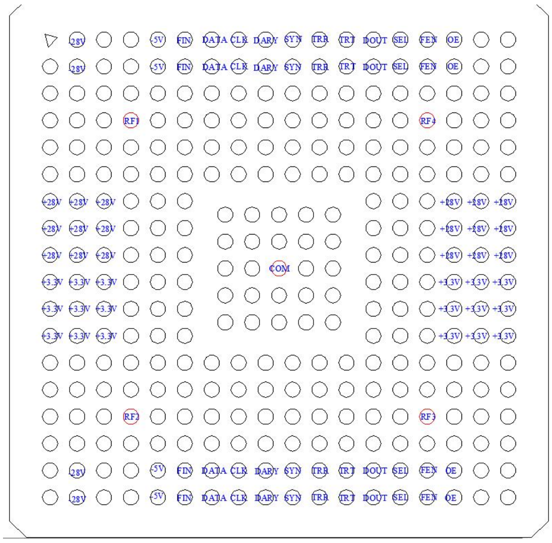
Outline Dimensions and Pad Arrangement Diagram







The pad arrangement is shown in the following figure.



Note: Unmarked pins are GND.

Serial Number	Symbol	Attribute	Level	Function Description

1	SEL	Input	TTL	Chip Select Signal, active at low level
2	DOUT	Output	TTL	Serial output of the status register, self - test signal
3	TRT	Input	TTL	Transmit external switch input
4	TRR	Input	TTL	Receive external switch input
5	SYN	Input	TTL	Write trigger signal for status data register 2, active at the rising edge
6	DARY	Input	TTL	Write trigger signal for status data register 1, active at the rising edge
7	CLK	Input	TTL	Clock signal input bit
8	DATA	Input	TTL	Serial data input bit of the status register
9	OE	Input	TTL	Reset enable signal
10	FIN	Input	TTL	Serial data input bit of the control register
11	FEN	Input	TTL	Serial input enable bit of the control register. Serial input is valid at low level, and FIN data is latched at the rising edge
12	-5V	Input		-5V voltage input
13	-28V	Input		-28V voltage input
14	+3.3V	Input		+3.3V voltage input
15	+28V	Input		+28V voltage input
16	RF1	Input/Output		Channel 1 RF input/output port
17	RF2	Input/Output		Channel 2 RF input/output port
18	RF3	Input/Output		Channel 3 RF input/output port
19	RF4	Input/Output		Channel 4 RF input/output port
20	COM	Input/Output		Common input/output port
Others	GND	Ground		Ground

Precautions

1. The module should be soldered to the board in a clean environment.
2. The bottom surface of the module is soldered with 400μm - diameter high - lead solder balls using a 183°C solder (Sn63Pb37).
3. The inside of the module can withstand a high temperature of 240°C. It is recommended to use Sn63Pb37 solder paste for SMT soldering of the module. After soldering, spray cleaning can be carried out, but ultrasonic cleaning is not allowed.
4. It is recommended to select a circuit board material with a small difference in thermal expansion coefficient from that of ceramics for the design of the circuit board on which the module is mounted. Infrared heating is not suitable for the repair of the module after it is mounted on the board.
5. There are electrostatic - sensitive components inside the module. During transportation and storage, it is packaged in a special anti - static sealed package. When soldering the module to the board, the personnel and equipment should have reliable anti - static measures. Do not open the package without anti - static measures. During the subsequent board - level and system - level testing and use of the module, electrostatic protection should be paid attention to.
6. The anti - static sealed package of the module when shipped should be removed only when it is to be mounted and used. Unused modules after unpacking should be stored in a dry cabinet and mounted and used within 4 weeks.
7. When the module is in transmit operation, the heat dissipation is high. It is recommended to adopt a top - cooling method.
8. There are DC - blocking capacitors inside the RX1, RX2, RX3, RX4, TX1, TX2, TX3, TX4 ports, and there is also a DC - blocking capacitor inside the COM port.
9. When designing the application circuit of the module, 0.01μF and 1μF ceramic filter capacitors should be connected in parallel to the ground near the +28V, +3.3V, and -5V pins of the module.
10. Since it is triggered by the rising edge, LD should be at a high level when there is no signal.
11. If there are any problems, please contact the marketing personnel in a timely manner.
12. The indicators described in this document are estimated values. The specific indicators shall be subject to actual measurement.